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Maria E. Provencio
Signature

Maria E. Provencio
Printed Name

Applicant	:	Jerome T. Chu, et al.
Application No.	:	09/964,227
Filed	:	September 26, 2001
Title	:	METHOD AND STRUCTURE FOR MODULAR, HIGHLY LINEAR MOS CAPACITORS USING NITROGEN IMPLANTATION
Grp./Div.	:	2822
Examiner	:	J. Vockrodt
Docket No.	:	D8143-00328

APPELLANTS' BRIEF

Commissioner for Patents
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December 8, 2003

Commissioner:

This is an appeal from the Final Rejection of the claims in the above-referenced application, as made in the Final Office action dated May 2, 2003.

1. REAL PARTY IN INTEREST

The real party in interest is Agere Systems Inc.

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the present appeal, that are known to Appellants or Appellants' attorney.

3. STATUS OF CLAIMS

Claims 1-19, 27 and 28 are pending in this application. Claims 19, 27 and 28 have been allowed and are not the subject of this appeal. Claims 11 and 14 have been objected to and are not the subject of this appeal. Claims 1-10, 12, 13 and 15-18 have been rejected. The rejection of each of claims 1-10, 12, 13 and 15-18, is hereby appealed.

4. STATUS OF AMENDMENTS AFTER FINAL REJECTION

No response and therefore no amendments were filed after the Final Office action of May 2, 2003.

5. SUMMARY OF INVENTION

The present invention provides MOS capacitors and methods for forming the same. The MOS capacitors of the present invention are formed over a silicon substrate and are advantageously highly linear. The high linearity is attributable to an increased capacitance density when measured per unit of silicon surface area. The increased capacitance density is due in part to a suitably thin capacitor dielectric.

The present invention provides for the economical formation of the highly linear MOS capacitors and is described generally in the specification from page 1, line 34 to page 9, line 11.

The invention relates to providing a silicon substrate and forming highly N-doped regions in the silicon substrate to serve as lower electrodes for MOS capacitors. In disclosed embodiments, nitrogen is introduced into the highly N-doped silicon substrate region to define capacitor regions, and the substrate is thermally oxidized. The presence of nitrogen in the N-doped region suppresses the enhanced growth of the thermal oxide film which would otherwise occur in the N-doped regions due to Fermi level oxidation enhancement. Thermal oxide formed under suppressed growth may serve as a capacitor dielectric having a thickness less than an oxide film simultaneously formed in other highly N-doped regions which do not include nitrogen.

The process of the present invention is highly integrable in the sequence of processing operations used to form semiconductor devices because the thermal oxidation process used to form the capacitor dielectric is also used to simultaneously form transistor gate oxides in other regions of the substrate. Preferably, the presence of nitrogen maintains the resistance of the highly N-doped silicon electrode at a low value, which reduces the effect of voltage on the capacitance and thereby produces a more linear capacitor. A top capacitor plate may be formed over the capacitor dielectric.

The present invention enables provision of highly linear MOS capacitors by suppressing the effects of enhanced Fermi level oxidation and allows the capacitor dielectric to be formed simultaneously with transistor gate oxides formed in other regions of the substrate.

6. ISSUES PRESENTED

The issues presented are whether the Examiner properly rejected the claims in the May 2, 2003 Office action.

The first issue presented is whether or not the Examiner properly rejected claims 1-3, 15-16 and 19 under 35 USC § 102(b), as being allegedly anticipated by U.S. Patent No. 5,904,575 to Ishida, hereinafter "Ishida." Appellants point out that claim 19 has been allowed (Final Office action, page 7 under "Allowable Subject Matter") and will not be addressed in the following Argument even though it was listed (apparently erroneously) among rejected claims in this section, though not discussed.

The second issue presented is whether or not the Examiner properly rejected claims 1-3, 15-16 and 19 under 35 USC § 103(a) as being allegedly unpatentable over Ishida in view of U.S. Patent No. 6,255,169 to Li, hereinafter "Li '169". Appellants again point out that claim 19 has been allowed and will not be addressed in the following argument.

The third issue presented is whether or not the Examiner properly rejected claims 5, 7, 9, 13 and 18 under 35 USC § 103(a) as being unpatentable over Ishida and Li '169 as applied to claims 1-3, 15-16 and 19 above, further in view of U.S. Patent No. 5,854,114 to Li, hereinafter "Li '144".

The fourth issue presented is whether or not the Examiner properly rejected claims 5, 6, 12 and 17 under 35 USC § 103(a) as being allegedly unpatentable over Ishida and Li '169 as applied to claims 1-3, 15-16 and 19 above, and further in view of U.S. Patent No. 5,750,428 to Chang, hereinafter "Chang".

The fifth issue presented is whether or not the Examiner properly rejected claims 4, 8 and 10 under 35 USC § 103(a) as being allegedly unpatentable over Ishida and Li '169 as applied to claims 1-3, 15-16 and 19 above, and further in view of U.S. Patent No. 5,942,780 to Barsan, hereinafter "Barsan".

7. GROUPING OF CLAIMS

Claim 1 is an independent claim and claims 2-10, 12, 13 and 15-18 depend, directly or indirectly from independent claim 1. Each of the rejected claims 1-10, 12, 13 and 15-18 are presented as standing separately as each of the dependent claims are considered to be separately patentable in combination with claim 1.

The complete set of rejected claims that are the subject of this appeal, is included in the Appendix (Section 9).

8. ARGUMENT

8A. Final Rejection of Claims 1-10, 12, 13 and 15-18.

In the final Office action dated May 2, 2003, claims 1-10, 12, 13 and 15-18 were rejected under 35 USC § 102(b) and under 35 USC § 103(a).

In particular, the Examiner rejected claims 1-3, 15-16 and 19 under 35 USC § 102(b) as being anticipated by Ishida (U.S. Patent No. 5,204,575). Claims 1-3, 15-16 and 19 were also rejected under 35 USC § 103(a) as being unpatentable over Ishida in view of Li '169 (U.S. Patent No. 6,255,169). Claims 5, 7, 9, 13 and 18 were rejected under 35 USC § 103(a) as being unpatentable over Ishida and Li '169 as applied to claims 1-3, 15-16 and 19, further in view of Li '114 (U.S. Patent No. 5,854,144). The Examiner further rejected claims 5, 6, 12 and 17 under 35 USC § 103(a) as being unpatentable over Ishida and Li '169 as applied to claims 1-3, 15-16 and 19, further in view of Chang (U.S. Patent No. 5,750428). Finally, claims 4, 8 and 10 were rejected by the Examiner under 35 USC § 103(a) as being unpatentable over Ishida and Li '169 as applied to claims 1-3, 15-16 and 19, further in view of Barsan (U.S. Patent No. 5,942,780).

Appellants respectfully point out that although claim 19 was rejected as above, claim 19 and its base claim 28 were also indicated as being allowable on page 7, fourth paragraph of the subject final Office action. As such, Appellants in good faith understand claim 19 to be allowed and allowed claim 19 will not be the subject of this appeal.

The final Office action of May 2, 2003 also included the Examiner's comments regarding previously filed arguments included in a response filed by the Appellants, as applicants on March 4, 2003. The 04 March 2003 response was filed responsive to an Office action dated November 4, 2002.

A Notice of Appeal was filed on August 8, 2003, by Appellants in response to the final Office action of May 2, 2003.

8B. Claims 1-3 and 15-16 are not Subject to Rejection Under 35 USC § 102(b) as being Anticipated by Ishida (U.S. Patent No. 5,904,575).

Independent claim 1 forms a **capacitor**. Ishida, in contrast, is not directed to capacitors or methods for forming capacitors.

In particular, claim 1 recites the feature of:

"introducing N-type dopant impurities into said semiconductor surface, thereby forming N-doped regions within said semiconductor surface"

"introducing nitrogen into at least one of said N-doped regions to form at least one **capacitor** region"; and

"forming a **capacitor** by forming a top capacitor placed over each **capacitor** region".

In stark contrast, the terms "capacitor" and "capacitance" appear nowhere in the Ishida reference, much less in the claims, because Ishida is simply not directed to a capacitor. Ishida is directed to a method for oxidizing a substrate and an EEPROM memory cell having a program junction region in a semiconductor substrate. One of ordinary skill in the art recognizes that an EEPROM, particularly the EEPROM disclosed in Ishida, is distinguished from a capacitor because the EEPROM includes a *tunnel oxide* through which electrons are transferred from a substrate to a floating gate of a transistor by Fowler-Nordheim tunneling. A capacitor is distinguished as its dielectric is designed to store charge on opposed plates disposed across an insulating dielectric and not to allow electrons to pass from one plate to another. The conductive components across the tunnel oxide in an EEPROM are for charge transfer whereas capacitor plates are for charge storage. Since Ishida does not disclose a capacitor, Ishida cannot and does not disclose a method for forming a capacitor.

More particularly, Ishida does not disclose "introducing N-type dopant impurities" or "forming N-doped regions" as recited in claim 1. Ishida further does not disclose "introducing nitrogen into [an] . . . N-doped region" or "forming a capacitor by forming a top capacitor placed over each capacitor region" also as recited claim 1. As such, the Examiner's rejection under 35 USC § 102(b) must be reversed.

The Examiner's assertion that Ishida forms a capacitor is an impermissibbly broad interpretation of the Ishida reference and is insufficient to support a rejection under 35 USC § 102(b) which has been interpreted as follows: A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The Examiner's application of 35 USC § 102(b) falls short of the requirements of 35 USC § 102(b) because Ishida does not disclose a capacitor or N-doped regions, much less forming a capacitor by forming a top capacitor placed over each capacitor region or introducing N-type dopant impurities into a semiconductor surface or introducing nitrogen into N-doped regions to form a capacitor region. Since the reference does not disclose the claimed features, the rejection under 35 USC § 102(b) is inappropriate. The EEPROM disclosed in Ishida is not a capacitor.

The Examiner simply examines Figure 1 of Ishida (attached as Exhibit A), picks conductive elements and a dielectric element, decides that in combination these features form a capacitor, then rejects the claims based on his constructive combination of these selected features. Appellants respectfully submit that this is impermissible under of 35 USC § 102(b). The Examiner arbitrarily designates floating gate 106a to be an upper electrode, tunnel oxide 130b to be a capacitor dielectric and program junction 110a to be a lower capacitor electrode even though these are not features of a capacitor and a tunnel oxide is distinguished from a capacitor dielectric for reasons set forth above. The EEPROM features, in combination, do not disclose a capacitor structure, much less the *claimed method for forming a capacitor*. Furthermore, the ability of a capacitor to store charge is a function of the voltage and size of the capacitor plates, the dielectric between the capacitor plates and the spatial arrangements of the features. An examination of Figure 1 of Ishida shows that the features alleged by the Examiner to form a "capacitor" would not function as a capacitor but, rather, would have any capacitance affected by other dielectrics, in particular oxide layer 130c, that are disposed between the structures that the Examiner alleges to be capacitor electrodes.

Based on the Examiner's selective identification of different features to be combined to form a capacitor that forms the basis for the rejection of *method* claim 1, it would appear to follow that any two conductive features in any structure that are separated by a dielectric which could be air, could serve as a capacitor, regardless of the actual functionality or construction of the device, and that such a capacitor could be used for the purposes of claim rejections under 35 USC § 102(b), and could be further extended to serve as a basis for rejecting method claims drawn to forming a capacitor. Appellants respectfully submit that this is an impermissible extension of 35 USC § 102(b).

In summary, Ishida does not disclose a capacitor, and therefore cannot disclose a method for forming a capacitor. Furthermore, the structure identified by the Examiner does not suggest a capacitor, and the Examiner improperly chose arbitrary features of Figure 1 to create a capacitor which is an improper application of 35 USC § 102(b). More particularly, Ishida does not disclose the above-cited method features recited in claim 1, as required for an anticipation rejection under 35 USC § 102(b).

Therefore, the rejection of independent claim 1, under 35 USC § 102(b) as being anticipated by Ishida, should be reversed. Claims 2, 3 and 15 and 16 each depend from independent claim 1 and therefore incorporate the distinguishing features of claim 1 and are similarly distinguished from Ishida.

Dependent claim 2 recites the feature that "forming a top capacitor plate comprises forming one of a conductive material and a semiconductor material". Claim 3 recites the feature that the "step of introducing nitrogen comprises ion implantation". Claim 15 recites the feature that the "step of introducing nitrogen includes introducing nitrogen into a first portion of the designated N-doped region, a second portion of said designated N-dope region not having nitrogen introduced therein" and dependent claim 16 recites the feature that the "semiconductor substrate comprises silicon and the oxide film comprises silicon dioxide". Appellants respectfully submit that, based on the patentability of claim 1, each of claims 2, 3, 15 and 16 is further patentable because the subject matter of the combination of claims 1 with claims 2, 3, 15 and 16 respectively, is distinguished from the art of record. Therefore the rejection of claims 1-3 and 15-16 under 35 USC § 102(b) as being anticipated by Ishida, should be reversed.

8C. Claims 1-3 and 15-16 are not Subject t Rejecti n Und r 35 USC § 103(a) as being Unpatentable Over Ishida in View of Li '169 (U.S. Patent No. 6,255,169).

In the subject final Office action, specifically on page 3, paragraph 7, claims 1-3, 15 and 16 and 19 were rejected under 35 USC § 103(a) as being unpatentable over U.S. Patent No. 5,904,575 ("Ishida") in view of U. S. Patent No. 6,255,169 ("Li '169"). Appellants respectfully submit that these rejections should be reversed based on the remarks set forth below.

The cited reference of Li '169 is directed to forming a tunnel oxide through which electrons are transferred from a substrate to a floating-gate electrode. Li '169 is not directed to a MOS capacitor. Li '169 merely discloses that the stress-induced-leakage current (SILC) of the inventive tunnel oxide could be performance tested by forming a series of capacitors. This further supports Appellants' above argument distinguishing an EEPROM from a capacitor. If these two structures were the same, there would be no need to form a diagnostic capacitor to diagnose the SILC performance of a tunnel oxide of an EEPROM. Li '169 does not disclose or suggest how to form such capacitors and does not propose how such capacitors could be MOS capacitors used to store charge in functioning semiconductor devices. Moreover, Li '169 is directed to method steps for forming an EEPROM cell. Li '169 does not disclose or suggest the above-cited method steps for forming a capacitor as in the claimed invention. Li '169 therefore does not make up for the above-stated deficiencies of Ishida.

Since independent claim 1 is directed to a capacitor and recites the method features highlighted above, independent claim 1 is distinguished from the cited reference of Ishida and Li '169, taken alone or in combination. Claims 2, 3 and 15 and 16 each depend from independent claim 1 and therefore incorporate the distinguishing features of claim 1 and are similarly distinguished from Ishida. Furthermore, claims 2, 3, 15 and 16 are separately patentable in combination with the features of claim 1 as set forth in section 8D, above. The Examiner's rejection of claims 1-3 and 15 and 16 as being unpatentable over Ishida in view of Li '169, should therefore be reversed.

8D. Claims 5, 7, 9, 13 and 18 are not Subject to Rejection Under 35 USC § 103(a)

In the Office action, specifically on page 5, third paragraph, claims 5, 7, 9, 13 and 18 were rejected under 35 USC § 103(a) as being unpatentable over Ishida and Li '169 as applied

to claims 1-3, 15-16 and 19 above, further in view of U.S. Patent No. 5,854,114 (hereinafter "Li '114"). Appellants respectfully submit that these claim rejections are in error for reasons set forth below.

Li '114 has apparently been relied upon for teaching a PRJ implant of phosphorus with a dose of about $1X10^{14}$ to $1x10^{16}$ ions/cm^2 and an energy of 50-100KeV. Li '114 is also directed to an EEPROM. Li '114 therefore does not make up for the above-stated deficiencies of Ishida and Li '169 and independent claim 1 is therefore distinguished from the references of Ishida, Li '169 and Li '114, taken alone or in combination.

Since claims 5, 7, 9, 13 and 18 each depend, directly or indirectly from independent claim 1 which is distinguished from the stated references for the reasons set forth above, claims 5, 7, 9, 13 and 18 are similarly distinguished from the references.

Dependent claim 5 recites the feature that the "step of thermally oxidizing includes forming said oxide film having said first thickness being less than 50% of said second thickness". Claim 7 depends from claim 1 and recites the features of "forming said N-doped regions to include an N-type impurity concentration which lies within the range of $10^{18}/cm^3$ to $10^{19}/cm^3$". Claim 9 recites the feature that the "step of thermally oxidizing includes forming said oxide film having a third thickness in [said] undoped regions, said third thickness being less than 50% of said second thickness" and claim 13 recites the feature that the N-type dopant impurity comprises "one of phosphorous and arsenic". Claim 18 depends from claim 17, which depends from claim 1, and claim 18 therefore includes the features that "thermally oxidizing comprises forming said oxide film such that said second thickness is greater than said first thickness by at least 80%" and that the step of thermally oxidizing includes "forming said oxide film having a third thickness in undoped regions of said silicon surface, said third thickness and first thickness being substantially equal". Based on the patentability of claim 1, each of claims 5, 7, 9, 13 and 18 is separately patentable because the subject matter of the combination of claim 1 with each of respective claims 5, 7, 9, 13 and 18, is respectively distinguished from the prior art. The rejections of claims 5, 7, 9, 13 and 18 under 35 USC § 103(a) as being unpatentable over Ishida and Li '169 and further in view of Li '114, should therefore be reversed.

8E. Claims 5, 6, 12 and 17 are n t Subject to Rejection Under 35 USC § 103(a)

In the Office action, specifically on page 5, last paragraph, claims 5, 6, 12 and 17 were rejected under 35 USC § 103(a) as being unpatentable over Ishida and Li '169 as applied to

claims 1-3, 15-16 and 19 above, further in view of U.S. Patent No. 5,750,428 (hereinafter "Chang"). These claim rejections are in error for reasons set forth below.

The cited reference of Chang has apparently been relied upon for providing a tunnel oxide and a gate oxide as a differentially grown oxide layer wherein the tunnel oxide is 50-100 angstroms and the gate oxide is 150-350 angstroms. Chang therefore does not make up for the above-stated deficiencies of Ishida and Li '169 and independent claim 1 is therefore distinguished from the references of Ishida, Li '169 and Chang, taken alone or in combination..

Since claims 5, 6, 12 and 17 each depend, directly or indirectly from independent claim 1 which is distinguished from the stated references for the reasons set forth above, claims 5, 6, 12 and 17 are similarly distinguished from the references of record.

Claim 6 recites the feature that the "first thickness is less than 55 angstroms and said second thickness lies within the range of 80-150 angstroms". Claim 12 recites the feature that "thermally oxidizing comprises furnace oxidation at a temperature ranging from 750°C to 950°C for a time ranging from 5 to 15 minutes" and claim 17 recites the feature that "thermally oxidizing comprises forming said oxide film such that said second oxide thickness is greater than said first oxide thickness by at least 80%". Based on the patentability of claim 1, each of claims 5, 6, 12 and 17 is also separately patentable because the subject matter of the combination of claim 1 with claims 5, 6, 12 and 17 respectively, is distinguished from the art of record. The rejections of claims 5, 6, 12 and 17 under 35 USC § 103(a) as being unpatentable over Ishida and Li '169 and further in view of Chang, should therefore be reversed.

8F. Claims 4, 8 and 10 are not Subject to Rejection Under 35 USC § 103(a)

In the Office action, specifically on page 6, fourth paragraph, claims 4, 8 and 10 were rejected under 35 USC § 103(a) as being unpatentable over Ishida and Li '169 as applied to claims 1-3, 15-16 and 19 above, further in view of U.S. Patent No. 5,942,780 ("Barsan"). Appellants respectfully submit that these claim rejections are in error for the reasons set forth below.

The cited reference of Barsan has apparently been relied upon for teaching a nitrogen implant dose of $15x10^{14}$ / cm^2 at range of 29-32KeV effective to suppress oxide growth and also for using a photoresist mask. Barsan is again directed to an EEPROM device. The cited reference of Barsan therefore does not make up for the above-stated deficiencies of a

combination of Ishida and Li '169. Independent claim 1 is therefore distinguished from the references of Ishida, Li '169 and Barsan, taken alone or in combination..

Claims 4, 8 and 10 each depend, directly or indirectly from independent claim 1 which is distinguished from the references for reasons set forth above, and therefore claims 4, 8, and 10 are similarly distinguished from the references of record. Claim 4 depends from claim 3 and includes the feature that the step of introducing nitrogen "comprises ion implantation" with an "implant energy within the range of 5-9 keV and an implant dosage which lies within the range of $10^{14}/cm^2$ $10^{15}/cm^2$". Claim 8 recites the feature that the "capacitor region includes a nitrogen density within the range of 10^{17} to $10^{19}/cm^3$" and claim 10 recites the feature that the process further comprises the step of "defining one capacitor region prior to said step of introducing nitrogen, said defining comprising forming a masking pattern in a photosensitive material". Appellants respectfully submit that, based on the patentability of claim 1, each of claims 4, 8 and 10 is also separately patentable because the subject matter of the combination of claim 1 with claims 4, 8 and 10, respectively, is distinguished from the prior art. Therefore, the Examiner's rejection of claims 4, 8 and 10 under 35 USC § 103(a) as being unpatentable over Ishida and Li '169 and further in view of Barsan, should be reversed.

8G. Comments Regarding Examiner's Response to Arguments.

In the final Office action of May 2, 2003, the Examiner provided commentary responsive to the arguments set forth in the appellants' previous response of March 4, 2003, beginning on page 8.

The Examiner alleges in this section that Ishida *inherently* teaches a capacitor. Appellants respectfully submit that inherency arguments are applicable to situations in which a structure is clearly disclosed and the characteristics of that structure are not explicitly stated. If a second structure is identical, then inherency principles might permissibly be used to establish that the second structure inherently includes the same characteristics. That is not the case here. At issue here is **not** whether two identical structures have the same characteristics; rather, the issue before us is the very nature of the structures.

Ishida does not disclose a capacitor. It is an impermissible application of 35 USC § 102(b) to designate arbitrary features of Ishida and then extend inherency principles to 1] consider that these features form a capacitor and 2] to allow this contrived structure to form the basis of the rejection of method claims directed to method steps not disclosed in the reference,

and used to form a capacitor. The term "capacitor" denotes a particular functional structure in a semiconductor device and the EEPROM, disclosed in Ishida and distinguished as above, is not a capacitor. Capacitors, by definition, store charge and are located and wired in a particular location to serve as a capacitor. Capacitors are clearly disclosed and claimed in the subject application and lacking from the Ishida reference.

The Examiner's allegations are clearly based on an improper theory of inherency. M.P.E.P. (Version 8) § 2112 recites in part,

> "To establish inherency, the extrinsic evidence **must make clear that the missing descriptive matter is necessarily present in the thing described in the reference**, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) [Emphasis added]

The capacitor features alleged by the Examiner to be inherent in Ishida are not "necessarily present in the thing described in the reference". One of ordinary skill in the art could readily construct the features disclosed in Ishida and NOT consider them for use in a capacitor as did Ishida. More importantly, one of ordinary skill in the art could readily provide the structure disclosed in Ishida and NOT use the claimed method steps for forming a capacitor. Finally, the "certain thing" that resulted from the given set of circumstances (features) is an EEPROM, not a capacitor. There is no basis for the examiner to claim that Ishida inherently discloses a capacitor.

8H. Conclusion.

In view of the foregoing remarks, Appellants submit that this application is in condition for allowance. Appellants respectfully request that the Board reverse the Examiner's rejection of all rejected, pending claims.

In accordance with 37 CFR §1.192(a), this Appeal Brief is being submitted in triplicate. Also enclosed is the fee for filing an Appeal Brief under 37 CFR §1.17(c) in the amount of $330 as well as a Petition for a Two Month Extension of Time and the appropriate fee.

Respectfully submitted,

DUANE MORRIS LLP

By 

Mark J. Marcelli
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619/744-2243

Attachments: Appendix (Section 9)

Exhibit A

APPENDIX

Claims Under Appeal

1. A process for forming a semiconductor product, comprising the steps of:

providing a semiconductor substrate having a semiconductor surface;

introducing N-type dopant impurities into said semiconductor surface, thereby forming N-doped regions within said semiconductor surface;

introducing nitrogen into at least one of said N-doped regions to form at least one capacitor region; and,

thermally oxidizing said substrate surface to form an oxide film on said semiconductor surface, said oxide film having a first thickness in said at least one capacitor region and a second thickness being greater than said first thickness in other portions of said N-doped regions; and

forming a capacitor by forming a top capacitor plate over each capacitor region.

2. The process as in claim 1, in which said forming a top capacitor plate comprises forming one of a conductive material and a semiconductor material.

3. The process as in claim 1, in which said step of introducing nitrogen comprises ion implantation.

4. The process as in claim 3, in which said step of introducing nitrogen includes an implant energy within the range of 5-9 keV and an implant dosage which lies within the range of 10^{14}/cm2 to 10^{15}/cm2.

5. The process as in claim 1, in which said step of thermally oxidizing includes forming said oxide film having said first thickness being less than 50% of said second thickness.

6. The process as in claim 1, in which said first thickness is less than 55 angstroms and said second thickness lies within the range of 80-150 angstroms.

7. The process as in claim 1, in which said step of introducing N-type dopant impurities includes forming said N-doped regions to include an N-type impurity concentration which lies within the range of 10^{18}/cm3 to 10^{19}/cm3.

8. The process as in claim 1, in which said capacitor region includes a nitrogen density within the range of 10^{17} to 10^{19}/cm3.

9. The process as in claim 1, in which semiconductor surface regions in which said N-type dopant impurities are not introduced, are designated undoped regions, and said step of thermally oxidizing includes forming said oxide film having a third thickness in said undoped regions, said third thickness being less than 50% of said second thickness.

10. The process as in claim 1, further comprising the step of defining said at least one capacitor region prior to said step of introducing nitrogen, said defining comprising forming a masking pattern in a photosensitive material.

12. The process as in claim 1, wherein said thermally oxidizing comprises furnace oxidation at a temperature ranging from 750°C to 950°C, for a time ranging from 5 to 15 minutes.

13. The process as in claim 1, wherein said N-type dopant impurity comprises one of phosphorous and arsenic.

15. The process as in claim 1, in which said step of introducing nitrogen includes introducing nitrogen into a first portion of a designated N-doped region, a second portion of said designated N-doped region not having nitrogen introduced therein.

16. The process as in claim 1, wherein said semiconductor substrate comprises silicon and said oxide film comprises silicon dioxide.

17. The process as in claim 1, wherein said thermally oxidizing comprises forming said oxide film such that said second thickness is greater than said first thickness by at least 80%.

18. The process as in claim 17, in which said step of thermally oxidizing includes forming said oxide film having a third thickness in undoped regions of said silicon surface, said third thickness and said first thickness being substantially equal.

MJM/mep

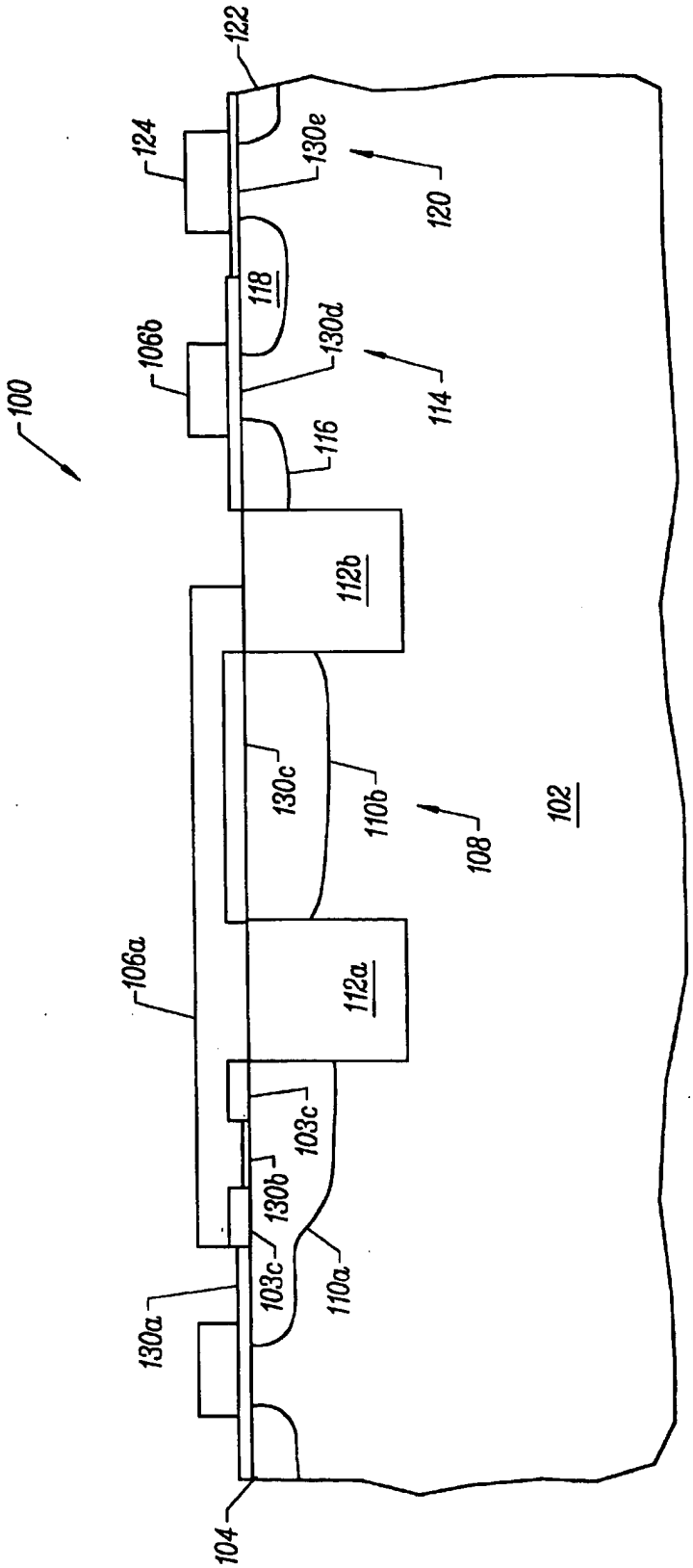
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FIG. 1